Register for Certification exam

Thank you for taking the Week 7 : Assignment 7.

Week 7 : Assignment 7

Your last recorded submission was on 2021-09-12, 20:50 IST

Due date: 2021-09-15, 23:59 IST.

1) Decimal equivalent of 11101011 represented in 2's complement format will be_____?

-21

1 point

2) Largest number that can be represented using 8-bit 1's complement representation will be_____

127

1 point

3) If we implement a half adder only with basic gates (AND, OR, NOT), then how many basic gates will be required?

a. 6
b. 5
c. 4
d. 3

1 point

- (●) a.
- ( ) b.
- ( ) c.
- ( ) d.

4) If the delay of each basic gates is "δ", and the inputs are available in both complemented and uncomplemented forms, the total delay required by SUM and CARRY outputs of a full adder is: *1 point*

a. 2 δ and 2 δ
b. 2 δ and 3 δ
c. 3 δ and 2 δ
d. 3 δ and 3 δ

- ○ a.
- ○ b.
- ◉ c.
- ○ d.

5) Which of the following statement(s) is/are true for carry lookahead adder? *1 point*

a. Addition can be carried out in constant time.
b. All carries can be generated in parallel.
c. The cost of carry lookahead circuit increase rapidly with increase in number of bits.
d. None of these.

- ☑ a.
- ☑ b.
- ☑ c.
- ☐ d.

6) Carry save adder consist of? *1 point*

a. Cascaded full adders.
b. Independent full adders.
c. Parallel adder in the last stage.
d. Carry select adders.
e. None of these.

- ☐ a.
- ☑ b.
- ☑ c.
- ☐ d.
- ☐ e.

7) In a 5-bit carry look-ahead adder, suppose we are adding two numbers A = (1, 0, 1, 1, 0) and B = (1, 0, 1, 1, 1). The carry generate and carry propagate signals will be: *1 point*

a. G = (1, 0, 1, 1, 0) and P = (1, 0, 1, 1, 1)
b. G = (1, 0, 1, 1, 0) and P = (0, 0, 1, 0, 1)
c. G = (1, 0, 1, 1, 0) and P = (0, 0, 0, 0, 1)
d. G = (1, 0, 1, 1, 0) and P = (1, 0, 0, 0, 1)

- ○ a.
- ○ b.
- ◉ c.
- ○ d.

8) Suppose we are multiplying (-9) x (12) using Booth's multiplier, where each number is represented in 5 bits. What will be the values of A (temporary register), and Q (multiplier) after third step? *1 point*

a. 00100, 00011
b. 01001, 00011
c. 00100, 10001
d. None of these.

- ○ a.
- ○ b.
- ◉ c.
- ○ d.

9) Which of the following statement(s) is/are true? *1 point*

a. Booth's multiplier is faster as compared to shift and add multiplication approach
b. Booth's multiplier inspects two bits of the multiplier at every step
c. Arithmetic right shift operation is used in Booth's multiplier.
d. None of these.

- ☑ a.
- ☑ b.
- ☑ c.
- ☐ d.

10) Suppose we are dividing 37/6 using restoring division method, where A and M are represented in 4 bits. What will be the value of A after the third step? *1 point*

a. 0000
b. 0100
c. 1011
d. 1110

- ○ a.
- ◉ b.
- ○ c.
- ○ d.

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers

Note: All these answers are confirmed from our side, we don't guarantee that you will get a 100% score. These are our own answers that we are sharing with you all. If you have any doubt that our answers are not correct then feel free to discuss (in-group) or do your own answer.

Most important: We don't promote any type of cheating, these answers are only for those students who are not able to do it on their own or need some help.